Instruction Set In Computer Architecture

Due to their low costs, low power consumption, and low heat generation, ARM processors are useful for light, portable, battery-powered devices, including smartphones, laptops, and tablet computers, as well as embedded systems. However, ARM processors are also used for desktops and servers, including Fugaku, the world's fastest supercomputer from 2020 to 2022. With over 230 billion ARM chips produced, since at least 2003, and with its dominance increasing every year, ARM is the most widely used family of instruction set architectures. 2b1c062223

Reduced instruction set computer Compared to the instructions given to a complex instruction set computer (CISC), a RISC computer might require more machine code in order to accomplish a task because the individual instructions perform simpler operations. The goal is to offset the need to process more instructions by increasing the speed of each instruction, in particular by implementing an instruction pipeline, which may be simpler to achieve given simpler instructions. In electronics and computer science, a reduced instruction set computer (RISC, pronounced "risk") is a computer architecture designed to simplify the individual In electronics and computer science, a reduced instruction set computer (RISC, pronounced "risk") is a computer architecture designed to simplify the individual instructions given to the computer to accomplish tasks 2b1c062223

== History == 2b1c062223

Comparison of instruction set architectures Both of these developments have helped to lower the cost of computers and to increase their applicability. A realization of an ISA is called An instruction set architecture (ISA) is an abstract model of a computer, also referred to as computer architecture. An ISA permits multiple implementations that may vary in performance, physical size, and monetary cost (among other things); because the ISA serves as the interface between software and hardware, software that has been written or compiled for an ISA can run on different implementations of the same ISA. For these reasons, the ISA is one of the most important abstractions in computing today. A realization of an ISA is called an implementation. An instruction set architecture (ISA) is an abstract model of a computer, also referred to as computer architecture. This has enabled binary compatibility between different generations of computers to be easily achieved, and the development of computer families 2b1c062223

Explicitly parallel instruction computing This was intended to allow simple performance scaling without resorting to higher clock frequencies. researchers at HP recognized that reduced instruction set computer (RISC) architectures were reaching a limit at one instruction per cycle. This paradigm is also called Independence architectures. [clarification needed] Explicitly parallel instruction computing (EPIC) is a term coined in 1997 by the HP–Intel alliance to describe a computing paradigm that researchers had been investigating since the early 1980s.

It was the basis for Intel and HP development of the Intel Itanium architecture, and HP later asserted that "EPIC" was merely an old term for the Itanium architecture. EPIC permits microprocessors to execute software instructions in parallel by using the compiler, rather than complex on-die circuitry, to control parallel instruction execution 2b1c062223

No instruction set computing No instruction set computing (NISC) is a computing architecture and compiler technology for designing highly efficient custom processors and hardware accelerators No instruction set computing (NISC) is a computing architecture and compiler technology for designing highly efficient custom processors and hardware accelerators by allowing a compiler to have low-level control of hardware resources 2b1c062223

The key operational concept of the RISC computer is that each instruction performs only one function (e.g., copy a value from memory to a register). The RISC computer usually has many (16 or 32) high-speed, general-purpose registers with a load–store architecture in which the instructions that perform arithmetic and tests operate only on the registers, and the instructions that access data in the main memory of the computer only load data from memory into registers or store data from registers into memory. The design of the CPU allows... 2b1c062223 The first documented computer architecture was in the correspondence between Charles Babbage and Ada Lovelace, describing the analytical engine. While building the computer Z1 in 1936, Konrad Zuse described in two patent applications for his future projects that machine instructions could be stored in the same storage used for data, i.e., the stored-program concept. Two other early and important examples are: 2b1c062223

One-instruction set computer The first carbon nanotube computer is a 1-bit one-instruction set computer (and has only 178 transistors). A one-instruction set computer (OISC), sometimes referred to as an ultimate reduced instruction set computer (URISC), is an abstract machine that uses A one-instruction set computer (OISC), sometimes referred to as an ultimate reduced instruction set computer (URISC), is an abstract machine that uses only one instruction – obviating the need for a machine language opcode. OISCs have been recommended as aids in teaching computer architecture and have been used as computational models in structural computing research. With a judicious choice for the single instruction and given arbitrarily many resources, an OISC is capable of being a universal computer in the same manner as traditional computers that have multiple instructions 2b1c062223

Instruction set architecture A device (i. CPU) that interprets instructions described by an ISA is an implementation of that ISA. Generally, the same ISA is used for a family of related CPU devices. An instruction set architecture (ISA) is an abstract model that defines the programmable interface of the CPU of a computer, defining how software interacts An instruction set architecture (ISA) is an abstract model that defines the programmable interface of the CPU of a computer, defining how software interacts with hardware. e 2b1c062223

ARM architecture family (stylised in lowercase as arm) is a family of RISC instruction set architectures for computer processors. Arm Holdings develops the instruction set architecture ARM (stylised in lowercase as arm) is a family of RISC instruction set architectures for

computer processors. Arm Holdings develops the instruction set architecture and licenses them to other companies, who build the physical devices that use the instruction set. It also designs and licenses cores that implement these instruction set architectures 2b1c062223

== Overview == 2b1c062223

Computer architecture Computer architecture also considers tradeoffs In computer science and computer engineering, a computer architecture is the conceptual design and operational structure of a computer system that define how component parts are organized and interact to execute programs efficiently. It covers the instruction set architecture, CPU microarchitecture, memory, and input/output systems. It covers the instruction set architecture, CPU microarchitecture, memory, and input/output systems. It is often a general description that ignores precise implementation details. details 2b1c062223

== Machine architecture == 2b1c062223 An ISA defines everything a machine language programmer needs to know in order to program a computer. What an ISA defines differs between ISAs; in general, ISAs define the supported data types, what state there is (such as the main memory and registers) and their semantics (such as the memory consistency and addressing modes), the instruction set (the set of machine instructions that... 2b1c062223 IBM continues to develop PowerPC microprocessor cores for use in their application-specific integrated circuit (ASIC) offerings. Many high volume applications embed PowerPC cores. 2b1c062223 Examples of CISC architectures include complex mainframe computers to simplistic microcontrollers where memory load and store operations are not separated from arithmetic instructions. Specific instruction set architectures that have been retroactively labeled CISC are System/360 through z/Architecture, the PDP-11 and VAX architectures, and many others. Well known microprocessors and microcontrollers that have also been labeled CISC in many academic publications include the Motorola 6800, 6809 and 68000 families; the Intel 8080, iAPX 432, x86 and 8051 families... 2b1c062223 In general, an ISA defines the instructions, data types, registers, and the programming interface for managing main memory such as addressing modes, virtual memory, and memory consistency mechanisms. The ISA also includes the input/output model of the programmable interface. 2b1c062223 NISC is a statically scheduled horizontal nanocoded architecture (SSHNA). The term "statically scheduled" means that the operation scheduling and hazard handling are done by a compiler. The term "horizontal nanocoded" means that NISC does not have any predefined instruction set or microcode. The compiler generates nanocodes which directly control functional units, registers and multiplexers of a given datapath. Giving low-level control to the compiler enables better utilization of datapath resources, which ultimately result in better performance. The benefits of NISC technology are: 2b1c062223 The ISA evolved into the PowerPC instruction set architecture and was itself deprecated in 1998, when IBM introduced the POWER3 processor that was mainly a 32/64-bit PowerPC processor but included IBM POWER architecture features for backwards compatibility. The original IBM POWER architecture was then abandoned. PowerPC evolved again into the Power ISA in 2006. 2b1c062223 The ISA was used for high-end IBM microprocessors during the early 1990s and were used in many of IBM's servers, minicomputers, workstations, and supercomputers. These processors are called POWER1

(RIOS-1, RIOS.9, RSC, RAD6000) and POWER2 (POWER2, POWER2+ and P2SC). 2b1c062223 An ISA specifies the behavior implied by machine code running on an implementation of that ISA in a fashion that does not depend on the characteristics of that implementation, providing binary compatibility between implementations. This enables multiple implementations of an ISA that differ in characteristics such as performance, physical size, and monetary cost (among other things), but that are capable of running the same machine code, so that a lower-performance, lower-cost machine can be replaced with a higher-cost, higher-performance machine without having to replace software... 2b1c062223 == Roots in VLIW == 2b1c062223 In a Turing-complete model, each memory location can store an arbitrary integer, and – depending on the mode, there may be arbitrarily many locations. The instructions themselves reside in memory as a sequence of such integers. 2b1c062223 One goal of EPIC was to move the complexity of instruction scheduling from the CPU hardware to the software compiler... 2b1c062223 There have been several generations of the ARM design. The original ARM1 used a 32-bit internal structure but had a 26-bit address space that limited it to 64 MB of main memory. This limitation was removed in the ARMv3 series, which has a 32-bit address space, and several additional generations up to ARMv7 remained... 2b1c062223 Computer architecture also considers tradeoffs between performance, cost, power, reliability, and security. 2b1c062223

IBM POWER architecture The name is an acronym for Performance Optimization With Enhanced RISC. The name is an acronym for Performance Optimization IBM POWER is a reduced instruction set computer (RISC) instruction set architecture (ISA) developed by IBM. IBM POWER is a reduced instruction set computer (RISC) instruction set architecture (ISA) developed by IBM 2b1c062223

By 1989, researchers at HP recognized that reduced instruction set computer (RISC) architectures were reaching a limit at one instruction per cycle. They began an investigation into a new architecture, later named EPIC. The basis for the research was VLIW, in which multiple operations are encoded in every instruction, and then processed by multiple execution units. 2b1c062223 There exists a class of universal computers with a single instruction based on bit manipulation such as bit copying or bit inversion. Since their memory model is finite, as is the memory structure used in real computers, those bit manipulation machines... 2b1c062223

Complex instruction set computer A complex instruction set computer (CISC /'sɪsk/) is a computer architecture in which single instructions can execute several low-level operations (such A complex instruction set computer (CISC) is a computer architecture in which single instructions can execute several low-level operations (such as a load from memory, an arithmetic operation, and a memory store) or are capable of multi-step operations or addressing modes within single instructions. The term was retroactively coined in contrast to reduced instruction set computer (RISC) and has therefore become something of an umbrella term for everything that is not RISC, where some of the most common differentiating factors of a RISC architecture are uniform instruction length, and strictly separate memory access instructions 2b1c062223

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